IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of: David C. CHAPMAN	
Serial No.: 09/421,437	Examiner: A. Thompson
Filing Date: October 19, 1999	Art Unit: 2825
For: APPROACH FOR ROUTING AN INTEGRATED CIRCUIT	

Honorable Commissioner for Patents
Washington, D.C. 20231

APPEAL BRIEF

Sir:

This Appeal Brief is submitted in support of the Notice of Appeal filed October 11, 2001.

I. REAL PARTY IN INTEREST

David C. Chapman is the real party in interest.

II. RELATED APPEALS AND INTERFERENCES

Appellants are unaware of any related appeals or interferences.

III. STATUS OF CLAIMS

Claims 1-67 are pending in this application. After the final Office Action mailed on July 11, 2001, Claims 1-6, 10-35, 39-53 and 57-67 stand finally rejected and are the subject of this

appeal. Claims 7-9, 36-38 and 54-56 stand as allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claim.

IV. STATUS OF AMENDMENTS

After the final Office Action, an amendment was filed by facsimile on September 10, 2001, to place Claim 21 in better form for consideration on appeal. As of the filing of this Appeal Brief, no correspondence has been received from the USPTO to indicate whether this amendment was entered. A copy of the amendment, as filed, is attached hereto at Tab 1.

V. SUMMARY OF THE INVENTION

Although it is practical for layout designers to construct small transistor-level circuits by hand, there are typically hundreds of variants used in an integrated circuit, with differing logic functions and/or electrical characteristics. Up to a person-year of labor is required to create all of these variants manually. A layout synthesis tool is a Computer-Aided Design (CAD) tool that constructs transistor level cells with little or no manual intervention. Area efficiency is of extreme importance because each of the cells will appear multiple times in the integrated circuit layout, so a layout synthesis tool must use area very efficiently even as it constructs layouts rapidly.

Routing an integrated circuit involves determining the placement of wires to electrically connect integrated circuit devices and cells so that the integrated circuit operates correctly. For small integrated circuits, routing can be performed by a circuit designer who manually adds new wires to make the necessary connections in the integrated circuit. Often, the designer repositions devices and cells to make room for the new wires. Although manual routing can provide

relatively compact designs, the manual approach is impractical for large integrated circuits containing millions of transistors.

For large integrated circuits, routing is performed automatically by a routing mechanism known as a "router" that is typically implemented as a software tool on a computer-aided design system. A router receives a data representation of the integrated circuit (a "layout") and the electrical connections to be made between devices and cells contained in the integrated circuit layout (a "netlist"). The router determines where to place new wires in the integrated circuit layout to make the specified connections. The placement of the new wires is important since the length and placement of the new wires can have a direct effect on the performance of the integrated circuit. After the router has determined where to place the new wires, the router updates the integrated circuit layout to reflect the new wires (Specification, Page 1, line 12 through Page 2, line 7).

According to one aspect of the invention, during global routing, hint polygons are added to the integrated circuit layout and strategy lists are generated for the new wires to be added. The hint polygons and strategy lists are used during detailed routing to aid in placing the new wires. If obstacle conflicts or insufficient space problems prevent the detailed routing of a new wire, then an obstacle resolution portion of global routing is used to resolve the obstacle conflict and/or provide additional space in the integrated circuit layout to route the new wires (Specification, Page 14, lines 16-23).

According to another aspect of the invention, a design rule check is performed on only an extended portion of a routing path (FIG. 10B and Specification, Page 37, line 22 through Page 39, line 7).

VI. ISSUES

1. Whether Claims 1-6, 10-20, 22, 24-35, 39-53 and 57-67 are unpatentable under 35 U.S.C. § 103(a) over "An Interactive Router for Analog IC Design," by Thorsten Adler and Jurgen Scheible, 1998 (hereinafter "*Adler*").

2. Whether Claim 21 is unpatentable under 35 U.S.C. § 103(a) over "A Practical Online Design Rule Checking System," by Goro Suzuki and Yoshio Okamura, 1990 (hereinafter "*Suzuki*").

3. Whether Claim 23 is unpatentable under 35 U.S.C. §103(a) over *Xiong*, U.S. Patent No. 5,550,748.

VII. GROUPING OF CLAIMS

It is respectfully submitted that Claims 1-6, 10-35, 39-53 and 57-67 do not fall or stand together and the following groupings are asserted:

GROUP 1: Claims 1-6, 11-15, 19, 20, 24-35, 40-44, 48, 49, 53, 58-62, 66 and 67

GROUP 2: Claims 10, 39 and 57

GROUP 3: Claims 16, 17, 45, 46, 63 and 64

GROUP 4: Claims 18, 47 and 65

GROUP 5: Claims 21 and 50

GROUP 6: Claims 22 and 51

GROUP 7: Claims 23 and 52

VIII. ARGUMENT

A. Introduction

It is well founded that to establish a *prima facie* case of obviousness under 35 U.S.C. §103(a), the references cited and relied upon must teach or suggest all the claim limitations. In addition, a sufficient factual basis to support the obviousness rejection must be proffered. *In re Freed*, 165 USPQ 570 (CCPA 1970); *In re Warner*, 154 USPQ 173 (CCPA 1967); *In re Lunsford*, 148 USPQ 721 (CCPA 1966). With respect to the present application, it is respectfully submitted that the references cited and relied upon do not in any way teach or suggest all the limitations of Claims 1-6, 10-35, 39-53 and 57-67. It is further submitted that a sufficient factual basis has not been proffered in the final Office Action mailed July 11, 2001 to support the rejections of Claims 1-6, 10-35, 39-53 and 57-67 under 35 U.S.C. §103 as being unpatentable over the references cited and relied upon for at least the reasons set forth hereinafter.

B. Claims 1-6, 11-15, 19, 20, 24-35, 40-44, 48, 49, 53, 58-62, 66 and 67 Are Patentable Over *Adler*

Claims 1-6, 11-15, 19, 20, 24-35, 40-44, 48, 49, 53, 58-62, 66 and 67 are directed to an approach for automatically routing an integrated circuit that requires the steps of:

> "receiving integrated circuit layout data that defines a set of two or more integrated circuit devices to be included in the integrated circuit;
> receiving integrated circuit connection data that specifies one or more electrical connections to be made between the integrated circuit devices;
> determining, based upon the integrated circuit layout data and the integrated circuit connection data, a set of one or more routing indicators that specify a set of one or more preferable intermediate routing locations through which a routing path is to be located to connect first and second integrated circuit devices from the set of two or more integrated circuit devices;
> determining, based upon the integrated circuit layout data, the integrated circuit connection data and the set of one or more routing indicators, the routing path between the first and second integrated circuit devices, wherein the routing path satisfies specified design criteria; and

updating the integrated circuit layout data to generate updated integrated circuit layout data that reflects the routing path between the first and second integrated circuit devices."

Claims 1-6, 11-15, 19, 20, 24-35, 40-44, 48, 49, 53, 58-62, 66 and 67 address the problem of how to automatically route an integrated circuit while avoiding problems appurtenant to conventional automated routing approaches.

Adler discloses an interactive analog IC design tool that uses an Analog Router (AR) and a Global Router (GR). The AR is implemented by a single layer maze router with a special oversizing algorithm and advanced treatment of arbitrary polygons. The oversizing algorithm enables placement of diagonal path segments near obstacle corners to increase layout density.

It is respectfully submitted that *Adler* does not in any way teach or suggest at least several of the steps required by Claims 1-6, 11-15, 19, 20, 24-35, 40-44, 48, 49, 53, 58-62, 66 and 67. For example, Claims 1-6, 11-15, 19, 20, 24-35, 40-44, 48, 49, 53, 58-62, 66 and 67 require "determining, based upon the integrated circuit layout data and the integrated circuit connection data, **a set of one or more routing indicators that specify a set of one or more preferable intermediate routing locations through which a routing path is to be located** to connect first and second integrated circuit devices from the set of two or more integrated circuit devices." Claims 1-6, 11-15, 19, 20, 24-35, 40-44, 48, 49, 53, 58-62, 66 and 67 also require "determining, based upon the integrated circuit layout data, the integrated circuit connection data and the set of one or more routing indicators, the routing path between the first and second integrated circuit devices, wherein the routing path satisfies specified design criteria." Neither of these required steps is in any way taught or suggested by *Adler*.

In *Adler*, there is no determination of intermediate routing locations or points of any kind through which a routing path is to be located. The tool of *Adler* uses a wavefront search with a cost function to determine a general routing path from a source to a destination with the lowest

cost. The wavefront search examines all points on the plane, leading outward from the starting point. During global routing, the GR generates tunnel polygons that define the area (grid points) in which the final routing can be performed by the AR. Hence, neither the wavefront search nor the use of tunnel polygons is in any way related to specifying "a set of one or more preferable intermediate routing locations through which a routing path is to be located," as required by Claims 1-6, 11-15, 19, 20, 24-35, 40-44, 48, 49, 53, 58-62, 66 and 67.

In the final Office Action, the Examiner asserted that the limitation of "determining, based upon the integrated circuit layout data, the integrated circuit connection data and the set of one or more routing indicators, the routing path between the first and second integrated circuit devices, wherein the routing path satisfies specified design criteria" required by Claims 1-6, 11-15, 19, 20, 24-35, 40-44, 48, 49, 53, 58-62, 66 and 67 is taught at Section 3.1 of *Adler* and more specifically, "the integer bits 21 and 29; additionally, this section discloses the use of a flag to indicate acceptable directions" (final Office Action, page 4).

Section 3.1 of *Adler* describes the use of a two-dimensional bitmap in the database of the GR that stores information about the layout grid. Each grid point has an associated 32 bit integer value that stores information about the grid point. In particular, "bits 21 to 29 store information whether it's forbidden to extend the wave from the current grid point to the neighboring grid points." Referring to the example in Figure 6, bits 21 to 29 of the integer value associated with grid point *a* are set to indicate that the wave cannot be propagated from point *a* into grid points *b*, *c*, *d*, *e* or *f*. Thus, the integer values specify directions where the wavefront search cannot be propagated and do not indicate locations through which a routing path is to be located.

In the example depicted in Figure 6 of *Adler*, the integer value associated with grid point *a* does not indicate whether the routing path is to be located from grid point *a* to the grid point to

the left, down, or down and left of grid point *a*, even though all three are available choices. Thus, the integer values associated with grid points maintained in the database of the GR do not in any way teach or suggest the step of "determining...a set of one or more preferable intermediate routing locations through which a routing path is to be located," as required by Claims 1-6, 11-15, 19, 20, 24-35, 40-44, 48, 49, 53, 58-62, 66 and 67.

For at least these reasons, it is respectfully submitted that Claims 1-6, 11-15, 19, 20, 24-35, 40-44, 48, 49, 53, 58-62, 66 and 67 are not in any way taught or suggested by *Adler* and that Claims 1-6, 11-15, 19, 20, 24-35, 40-44, 48, 49, 53, 58-62, 66 and 67 are therefore patentable over *Adler*.

C. Claims 10, 39 and 57 Are Patentable Over *Adler*

It is respectfully asserted that Claims 10, 39 and 57 are separately patentable from Claims 1-6, 11-15, 19, 20, 24-35, 40-44, 48, 49, 53, 58-62, 66 and 67 because Claims 10, 39 and 57 contain limitations that are both not required by Claims 1-6, 11-15, 19, 20, 24-35, 40-44, 48, 49, 53, 58-62, 66 and 67 and are not in any way taught or suggested by *Adler*. Claims 10, 39 and 57 require the additional limitations of:

> "wherein determining the routing path between the first and second integrated circuit devices includes
> identifying one or more obstacles that block the routing path, and
> determining, based upon the integrated circuit layout data, the integrated circuit connection data and the set of one or more routing indicators, the routing path between the first and second integrated circuit devices, wherein the routing path is routed from the second integrated circuit device to the first integrated circuit device."

Claims 10, 39 and 57 are directed to avoiding obstacles by routing from the second integrated circuit device to the first integrated circuit device, instead of from the first integrated circuit device to the second integrated circuit device, as is conventionally done. This approach is

not in any way taught or suggested by *Adler*. Section 2.3 of *Adler* discloses "direction preserving backtracking from target to source and path generation is similar to Lee's algorithm." Conventional Lee algorithms use a wavefront search to identify a set of all possible routing paths from a source to a target. By definition, the wavefront search starts at a particular point and proceeds only outward. Backtracking is then used to select a path from the set of all possible routing paths that has the least cost. Thus, the backtracking described in *Adler* refers to backtracking over routes that have already been established (routed) from the source to the target, but not actually routing from a destination to a source, as is required by Claims 10, 39 and 57. There is absolutely no mention or suggestion in *Adler* whatsoever of routing from a target to a source to avoid obstacles.

In the final Office Action, the Examiner asserted that the steps required by Claims 10, 39 and 57 are taught or suggested by the text in Sections 3.1 and 3.3 of *Adler*. Section 3.1 describes aspects of the Global Router (GR) database including the use of the two-dimensional bitmap and issues relating to overlapping polygons, and Section 3.3 describes path generation by the GR and the Area Router (AR). There is nothing in either Section 3.1 or Section 3.3 of *Adler* that in any way teaches or suggests avoiding obstacles by routing from the target to the source, as is required by Claims 10, 39 and 57. For at least these reasons, it is respectfully submitted that Claims 10, 39 and 57 are not in any way taught or suggested by *Adler* and are therefore patentable over *Adler*.

D. Claims 16, 17, 45, 46, 63 and 64 Are Patentable Over *Adler*

It is respectfully asserted that Claims 16, 17, 45, 46, 63 and 64 are separately patentable from Claims 1-6, 11-15, 19, 20, 24-35, 40-44, 48, 49, 53, 58-62, 66 and 67 because Claims 16, 17, 45, 46, 63 and 64 contain limitations that are both not required by Claims 1-6, 11-15, 19, 20,

24-35, 40-44, 48, 49, 53, 58-62, 66 and 67 and are not in any way taught or suggested by *Adler*. Claims 16, 17, 45, 46, 63 and 64 require the additional limitations of:

> "performing one or more design rule checks on one or more portions of the routing path as the routing path is being determined."

Conventional layout synthesis tools normally provide some type of design rule checking to ensure that a layout satisfies a set of design rules. Design rule checking is conventionally performed on an entire layout as a separate phase in layout synthesis. Claims 16, 17, 45, 46, 63 and 64 require "on-the-fly" design rule checking on "one or more portions of the routing path as the routing path is being determined."

Adler mentions design rule checking generally, but does not in any way teach or suggest performing design rule checking "on one or more portions of the routing path as the routing path is being determined," as is required by Claims 16, 17, 45, 46, 63 and 64. In the final Office Action, the Examiner asserted that the additional steps required by Claims 16, 17, 45, 46, 63 and 64 are taught or suggested by the Abstract, Figures 1 and 2 and Sections 2.1 – 2.2.2 of *Adler*. These portions of *Adler*, however, teach or suggest only design rule checking generally and not the "on-the-fly" design rule checking required by Claims 16, 17, 45, 46, 63 and 64. For at least these reasons, it is respectfully submitted that Claims 16, 17, 45, 46, 63 and 64 are not in any way taught or suggested by *Adler* and are therefore patentable over *Adler*.

E. Claims 18, 47 and 65 Are Patentable Over *Adler*

It is respectfully asserted that Claims 18, 47 and 65 are separately patentable from Claims 1-6, 11-15, 19, 20, 24-35, 40-44, 48, 49, 53, 58-62, 66 and 67 because Claims 18, 47 and 65 contain limitations that are both not required by Claims 1-6, 11-15, 19, 20, 24-35, 40-44, 48, 49,

53, 58-62, 66 and 67 and are not in any way taught or suggested by *Adler*. Claims 18, 47 and 65 require determining the routing path between the first and second integrated circuit devices by:

> "extending the routing path a specified amount to generate an extended portion of the routing path, and
> selectively performing a design rule check on only the extended portion of the routing path"

Adler describes design rule checking generally, but does not in any way teach or suggest the use of selective design rule checking "on only the extended portion of the routing path," as is required by Claims 18, 47 and 65. To the extent that *Adler* discloses design rule checking, it is in the context of performing design rule checking on an entire layout, after the layout has been determined. There is no mention or suggestion in *Adler* whatsoever of performing selective design rule checking on an extended portion of a routing path as the routing path is being generated.

In the final Office Action, the Examiner asserted that the additional steps required by Claims 18, 47 and 65 are taught or suggested by the Abstract, Figures 1 and 2 and Sections 2.1 – 2.2.2 of *Adler*. It is respectfully submitted, however, that these portions of *Adler* teach or suggest only design rule checking generally and not the selective design rule checking required by Claims 18, 47 and 65. For at least these reasons, it is respectfully submitted that Claims 18, 47 and 65 are not in any way taught or suggested by *Adler* and are therefore patentable over *Adler*.

F. Claims 21 and 50 Are Patentable Over *Suzuki*

It is respectfully asserted that Claims 21 and 50 are separately patentable from Claims 1-6, 11-15, 19, 20, 24-35, 40-44, 48, 49, 53, 58-62, 66 and 67 because Claims 21 and 50 contain

limitations that are both not required by Claims 1-6, 11-15, 19, 20, 24-35, 40-44, 48, 49, 53, 58-62, 66 and 67 and are not in any way taught or suggested by *Suzuki*.

Claims 21 and 50 are directed to an approach for automatically verifying an integrated circuit layout that requires:

> "receiving integrated circuit layout data that defines a set of two or more layout objects contained in the integrated circuit layout;
> performing a first design rule check on a layout object from the set of two or more layout objects by evaluating the layout object against specified design criteria;
> changing one or more values defined by the specified design criteria to generate updated specified design criteria, wherein the changing of the one or more values is performed after a specified amount of time has elapsed and is made with respect to either the layout object or one or more other layout objects from the set of two or more layout objects; and
> performing a second design rule check on the layout object by evaluating the layout object against the updated specified design criteria."

The approaches recited in Claims 21 and 50 require a time-varying design rule check for verifying an integrated circuit layout. One or more values defined by specified design criteria used for a design rule check are varied over time with respect to one or more layout objects contained in the integrated circuit layout.

Suzuki discloses a conventional incremental design rule checking system that selectively applies all or a portion of a set of design rule checks to portions of an integrated circuit layout. While the Applicant agrees with the Examiner's assertion that the incremental design rule checks in *Suzuki* may be performed repeatedly, *Suzuki* does not in any way teach or suggest selectively changing one or more values defined by the specified design criteria over time with respect to a layout object and using the changed values in a subsequent design rule check. It is therefore respectfully submitted that Claims 21 and 50 are not in any way taught or suggested by *Suzuki* and are therefore patentable over *Suzuki*.

G. Claims 22 and 51 Are Patentable Over *Adler*

It is respectfully asserted that Claims 22 and 51 are separately patentable from Claims 1-6, 11-15, 19, 20, 24-35, 40-44, 48, 49, 53, 58-62, 66 and 67 because Claims 22 and 51 contain limitations that are both not required by Claims 1-6, 11-15, 19, 20, 24-35, 40-44, 48, 49, 53, 58-62, 66 and 67 and are not in any way taught or suggested by *Adler*.

Claims 22 and 51 are directed to an approach for automatically routing an integrated circuit that requires the steps of:

> "receiving integrated circuit layout data that defines a set of two or more integrated circuit devices to be included in the integrated circuit;
> receiving integrated circuit connection data that specifies one or more electrical connections to be made between the integrated circuit devices;
> determining, based upon the integrated circuit layout data and the integrated circuit connection data, a set of two or more join points that are to be electrically connected, wherein each join point from the set of two or more join points has an associated set of specified design criteria that control attachment of routing paths thereto;
> determining, based upon the integrated circuit layout data and the set of two or more join points, one or more routing paths to connect the set of two or more join points, wherein the one or more routing paths satisfy the specified design criteria associated with the set of two or more join points; and
> updating the integrated circuit layout data to generate updated integrated circuit layout data that reflects the one or more routing paths."

The approach for automatically routing an integrated circuit recited in Claims 22 and 51 requires the use of join point-specific design criteria to control the attachment of routing paths to join points. Using join point-specific design criteria allows relatively greater flexibility than conventional approaches that use global design criteria. For example, using join point-specific design criteria allows design rules to be selectively applied to join points and not to, for example, routing paths, other layout features or other join points.

Adler discloses using a cost function to select a particular path from the source to target and does not in any way teach or suggest using join point-specific design criteria to

automatically route an integrated circuit. In the final Office Action, the Examiner asserted that the approaches recited in Claims 22 and 51 are taught or suggested by Sections 2.2 – 2.4 of *Adler*. These portions of *Adler* discuss how a wire is connected to points on the source and target, but there is no mention of using a set of specified design criteria to control the attachment of the wire to these points on the source and target, as is required by Claims 22 and 51. For at least these reasons, it is respectfully submitted that Claims 22 and 51 are not in any way taught or suggested by *Adler* and are therefore patentable over *Adler*.

H. Claims 23 and 52 Are Patentable Over *Xiong*

It is respectfully asserted that Claims 23 and 52 are separately patentable from Claims 1-6, 11-15, 19, 20, 24-35, 40-44, 48, 49, 53, 58-62, 66 and 67 because Claims 23 and 52 contain limitations that are both not required by Claims 1-6, 11-15, 19, 20, 24-35, 40-44, 48, 49, 53, 58-62, 66 and 67 and are not in any way taught or suggested by *Xiong*.

Claims 23 and 52 are directed to an approach for automatically routing an integrated circuit that requires the steps of:

> "receiving integrated circuit layout data that defines a set of two or more integrated circuit devices to be included in the integrated circuit;
> receiving integrated circuit connection data that specifies one or more electrical connections to be made between the integrated circuit devices;
> determining, based upon the integrated circuit layout data and the integrated circuit connection data, a routing path between first and second integrated circuit devices that satisfies specified design criteria, wherein determining the routing path between the first and second integrated circuit devices includes
> determining whether the distance to be routed for a portion of the routing path exceeds a specified distance, and
> if the distance to be routed for the portion of the routing path does not exceed the specified distance, then routing the portion of the routing path in a single step; and
> updating the integrated circuit layout data to generate updated integrated circuit layout data that reflects the routing path between the first and second integrated circuit devices."

The approach for automatically routing an integrated circuit recited in Claims 23 and 52 requires that a portion of a routing path be extended in a single step by an amount that does not exceed a specified distance. This approach is particularly useful in tight routing situations where the distance to be routed is so short that independent bends cannot be made, the selection of connection locales impacts the feasibility of routing or the remaining un-routed stretch after moving out from a join point is too short to add bends. In addition, construction of an entire feasible route in a single step allows error recovery mechanisms to make better decisions as to what should be removed. Otherwise, the recovery mechanism may have only short routing stubs as guidance.

In the final Office Action the Examiner asserted that all of the limitations required by Claims 23 and 52 are taught by *Xiong* at Col. 2, line 44 through Col. 3, line 13 and in FIGS. 3 and 4, except for the final step of "updating the integrated circuit layout data to generate updated integrated circuit layout data that reflects the routing path between the first and second integrated circuit devices." The approach described in *Xiong* for routing and integrated circuit layout ensures that time delay constraints are satisfied. A search region is defined that satisfies specified time delay constraints. Connections are then routed to available locations within the search region. More specifically, *Xiong* teaches selecting the shortest delay path from a source pin of the signal net passing through a free point to a sink pin of the signal net and then routing the signal net along a routed path that includes the shortest delay path. Nothing in *Xiong* in any way teaches or suggests "determining whether the distance to be routed for a portion of the routing path exceeds a specified distance, and if the distance to be routed for the portion of the routing path does not exceed the specified distance, then routing the portion of the routing path

in a single step," as is required by Claims 23 and 52. For at least these reasons, it is respectfully submitted that Claims 23 and 52 are patentable over *Xiong*.

IX. CONCLUSION AND PRAYER FOR RELIEF

Based on the foregoing, it is respectfully submitted that the rejections of Claims 1-6, 10-35, 39-53 and 57-67 under 35 U.S.C. § 103 lacks the requisite factual and legal bases. Appellants therefore respectfully request that the Honorable Board reverse the rejections of Claims 1-6, 10-35, 39-53 and 57-67 under 35 U.S.C. § 103 over the references cited and relied upon.

Respectfully submitted,

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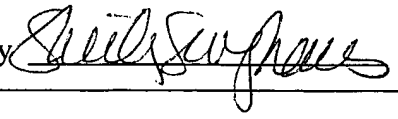
on February 11, 2002 by 

CLAIMS APPENDIX

1. A method for automatically routing an integrated circuit, the method comprising the computer-implemented steps of:

receiving integrated circuit layout data that defines a set of two or more integrated circuit devices to be included in the integrated circuit;

receiving integrated circuit connection data that specifies one or more electrical connections to be made between the integrated circuit devices;

determining, based upon the integrated circuit layout data and the integrated circuit connection data, a set of one or more routing indicators that specify a set of one or more preferable intermediate routing locations through which a routing path is to be located to connect first and second integrated circuit devices from the set of two or more integrated circuit devices;

determining, based upon the integrated circuit layout data, the integrated circuit connection data and the set of one or more routing indicators, the routing path between the first and second integrated circuit devices, wherein the routing path satisfies specified design criteria; and

updating the integrated circuit layout data to generate updated integrated circuit layout data that reflects the routing path between the first and second integrated circuit devices.

2. The method as recited in Claim 1, wherein determining the routing path includes determining, based upon the integrated circuit layout data, the integrated circuit

connection data, bias direction criteria and straying limit criteria, the routing path between the first and second integrated circuit devices, wherein the bias direction criteria specifies a preferred routing direction for a routing path between first and second integrated circuit devices from the set of two or more integrated circuit devices and the straying limit criteria defines a routing region in which the routing path between the first and second integrated circuit devices may be placed.

3. The method as recited in Claim 1, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

determining, based upon the integrated circuit layout data, the integrated circuit connection data and the one or more obstacles, one or more additional routing indicators that specify one or more preferable routing locations through which the routing path is to be located to avoid the one or more obstacles, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the one or more additional routing indicators, the routing path between the first and second integrated circuit devices.

4. The method as recited in Claim 1, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

changing specified straying limit criteria that defines a routing region in which the routing path between the first and second integrated circuit devices may be placed to generate changed specified straying limit criteria that defines a modified routing region, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the changed specified straying limit criteria, the routing path between the first and second integrated circuit devices.

5. The method as recited in Claim 1, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

determining a set of one or more layer changes to allow the routing path to avoid the one more obstacles, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the set of one or more layer changes, the routing path between the first and second integrated circuit devices.

6. The method as recited in Claim 1, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

determining a set of one or more bends to be included in the routing path to avoid the one more obstacles, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the set of one or more bends, the routing path between the first and second integrated circuit devices.

7. The method as recited in Claim 1, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

determining one or more portions of the routing path to be ripped up and rerouted, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the one or more portions of the routing path to be ripped up and rerouted, the routing path between the first and second integrated circuit devices.

8. The method as recited in Claim 7, wherein determining the routing path between the first and second integrated circuit devices further includes

determining one or more portions of one or more other routing paths to be ripped up and rerouted, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators, the one or more portions of the routing path to be ripped up and rerouted and the one or more

portions of the one or more other routing paths to be ripped up and rerouted, the routing path between the first and second integrated circuit devices.

9. The method as recited in Claim 1, wherein determining the routing path between the first and second integrated circuit devices further includes

identifying one or more obstacles that block the routing path,

determining one or more portions of one or more other routing paths to be ripped up and rerouted, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the one or more portions of the one or more other routing paths to be ripped up and rerouted, the routing path between the first and second integrated circuit devices.

10. The method as recited in Claim 1, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data and the set of one or more routing indicators, the routing path between the first and second integrated circuit devices, wherein the routing path is routed from the second integrated circuit device to the first integrated circuit device.

11. The method as recited in Claim 1, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

determining one or more locations to employ corner clipping to provide additional space for the routing path, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the one or more locations to employ corner clipping, the routing path between the first and second integrated circuit devices.

12. The method as recited in Claim 1, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

determining one or more integrated circuit layout objects to be moved to provide additional space for the routing path, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and moving the one or more integrated circuit layout objects, the routing path between the first and second integrated circuit devices.

13. The method as recited in Claim 1, wherein determining the routing path between the first and second integrated circuit devices includes

examining data that indicates whether changes can be made to one or more layout objects defined by the integrated circuit layout data to accommodate the routing of the routing path, and

if the data indicates that changes can be made to the one or more layout objects defined by the integrated circuit layout data to accommodate the routing of the routing path, then

making one or more changes to the one or more layout objects defined by the integrated circuit layout data, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the one or more changes made to the one or more layout objects, the routing path between the first and second integrated circuit devices.

14. The method as recited in Claim 13, further comprising generating data that specifies the one or more changes made to the one or more layout objects.

15. The method as recited in Claim 1, wherein determining the routing path between the first and second integrated circuit devices includes

determining a set of one or more routing targets to which the routing path is to be routed, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the set of one or

more routing targets, the routing path between the first and second integrated circuit devices.

16. The method as recited in Claim 1, wherein determining the routing path between the first and second integrated circuit devices includes performing one or more design rule checks on one or more portions of the routing path as the routing path is being determined.

17. The method as recited in Claim 16, further comprising performing a design rule check on the updated integrated circuit layout data, wherein the design rule check does not check one or more layout objects previously checked during determination of the routing path.

18. The method as recited in Claim 1, wherein determining the routing path between the first and second integrated circuit devices includes

extending the routing path a specified amount to generate an extended portion of the routing path, and

selectively performing a design rule check on only the extended portion of the routing path.

19. The method as recited in Claim 1, wherein all attachment and bend angles defined by the updated integrated circuit layout data are multiples of ninety degrees.

20. The method as recited in Claim 1, wherein one or more attachment or bend angles defined by the updated integrated circuit layout data are multiples of other than ninety degrees.

21. A method for automatically verifying an integrated circuit layout, the method comprising the computer-implemented steps of:

receiving integrated circuit layout data that defines a set of two or more layout objects contained in the integrated circuit layout;

performing a first design rule check on a layout object from the set of two or more layout objects by evaluating the layout object against specified design criteria;

changing one or more values defined by the specified design criteria to generate updated specified design criteria, wherein the changing of the one or more values is performed after a specified amount of time has elapsed and is made with respect to either the layout object or one or more other layout objects from the set of two or more layout objects; and

performing a second design rule check on the layout object by evaluating the layout object against the updated specified design criteria.

22. A method for automatically routing an integrated circuit, the method comprising the computer-implemented steps of:

receiving integrated circuit layout data that defines a set of two or more integrated circuit devices to be included in the integrated circuit;

receiving integrated circuit connection data that specifies one or more electrical connections to be made between the integrated circuit devices;

determining, based upon the integrated circuit layout data and the integrated circuit connection data, a set of two or more join points that are to be electrically

connected, wherein each join point from the set of two or more join points has an associated set of specified design criteria that control attachment of routing paths thereto;

determining, based upon the integrated circuit layout data and the set of two or more join points, one or more routing paths to connect the set of two or more join points, wherein the one or more routing paths satisfy the specified design criteria associated with the set of two or more join points; and

updating the integrated circuit layout data to generate updated integrated-circuit layout data that reflects the one or more routing paths.

23. A method for automatically routing an integrated circuit, the method comprising the computer-implemented steps of:

receiving integrated circuit layout data that defines a set of two or more integrated circuit devices to be included in the integrated circuit;

receiving integrated circuit connection data that specifies one or more electrical connections to be made between the integrated circuit devices;

determining, based upon the integrated circuit layout data and the integrated circuit connection data, a routing path between first and second integrated circuit devices that satisfies specified design criteria, wherein determining the routing path between the first and second integrated circuit devices includes

determining whether the distance to be routed for a portion of the routing path exceeds a specified distance, and

if the distance to be routed for the portion of the routing path does not exceed the specified distance, then routing the portion of the routing path in a single step; and

updating the integrated circuit layout data to generate updated integrated circuit layout data that reflects the routing path between the first and second integrated circuit devices.

24. A computer-readable medium carrying one or more sequences of one or more instructions for automatically routing an integrated circuit, the one or more sequences of one or more instructions including instructions which, when executed by one or more processors, cause the one or more processors to perform the steps of:

receiving integrated circuit layout data that defines a set of two or more integrated circuit devices to be included in the integrated circuit;

receiving integrated circuit connection data that specifies one or more electrical connections to be made between the integrated circuit devices;

determining, based upon the integrated circuit layout data and the integrated circuit connection data, a set of one or more routing indicators that specify a set of one or more preferable intermediate routing locations through which a routing path is to be located to connect first and second integrated circuit devices from the set of two or more integrated circuit devices;

determining, based upon the integrated circuit layout data, the integrated circuit connection data and the set of one or more routing indicators, the routing path

between the first and second integrated circuit devices, wherein the routing path satisfies specified design criteria; and

updating the integrated circuit layout data to generate updated integrated circuit layout data that reflects the routing path between the first and second integrated circuit devices.

25. The computer-readable medium as recited in Claim 24, wherein determining the routing path includes determining, based upon the integrated circuit layout data, the integrated circuit connection data, bias direction criteria and straying limit criteria, the routing path between the first and second integrated circuit devices, wherein the bias direction criteria specifies a preferred routing direction for a routing path between first and second integrated circuit devices from the set of two or more integrated circuit devices and the straying limit criteria defines a routing region in which the routing path between the first and second integrated circuit devices may be placed.

26. The computer-readable medium as recited in Claim 24, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

determining, based upon the integrated circuit layout data, the integrated circuit connection data and the one or more obstacles, one or more additional routing indicators that specify one or more preferable routing locations through which the routing path is to be located to avoid the one or more obstacles, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the one or more additional routing indicators, the routing path between the first and second integrated circuit devices.

27. The computer-readable medium as recited in Claim 24, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

changing specified straying limit criteria that defines a routing region in which the routing path between the first and second integrated circuit devices may be placed to generate changed specified straying limit criteria that defines a modified routing region, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the changed specified straying limit criteria, the routing path between the first and second integrated circuit devices.

28. The computer-readable medium as recited in Claim 24, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

determining a set of one or more layer changes to allow the routing path to avoid the one more obstacles, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the set of one or more layer changes, the routing path between the first and second integrated circuit devices.

29. A system for automatically routing an integrated circuit, the system comprising:

a data storage mechanism having stored therein

integrated circuit layout data that defines a set of two or more integrated circuit devices to be included in the integrated circuit, and

integrated circuit connection data that specifies one or more electrical connections to be made between the integrated circuit devices; and

a routing mechanism communicatively coupled to the data storage mechanism, the routing mechanism being configured to

determine, based upon the integrated circuit layout data and the integrated circuit connection data, a set of one or more routing indicators that specify a set of one or more preferable intermediate routing locations through which a routing path is to be located to connect first and second integrated circuit devices from the set of two or more integrated circuit devices,

determine, based upon the integrated circuit layout data, the integrated circuit connection data and the set of one or more routing indicators, the routing path between the first and second integrated circuit devices, wherein the routing path satisfies specified design criteria, and

update the integrated circuit layout data to generate updated integrated circuit layout data that reflects the routing path between the first and second integrated circuit devices.

30. The system as recited in Claim 29, wherein the routing mechanism is further configured to determine the routing path by determining, based upon the integrated circuit layout data, the integrated circuit connection data, bias direction criteria and straying limit criteria, the routing path between the first and second integrated circuit devices, wherein the bias direction criteria specifies a preferred routing direction for a routing path between first and second integrated circuit devices from the set of two or more integrated circuit devices and the straying limit criteria defines a routing region in which the routing path between the first and second integrated circuit devices may be placed.

31. The system as recited in Claim 29, wherein the routing mechanism is further configured to determine the routing path between the first and second integrated circuit devices by

identifying one or more obstacles that block the routing path,

determining, based upon the integrated circuit layout data, the integrated circuit connection data and the one or more obstacles, one or more additional routing indicators that specify one or more preferable routing locations through which the routing path is to be located to avoid the one or more obstacles, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the one or more

additional routing indicators, the routing path between the first and second integrated circuit devices.

32. The system as recited in Claim 29, wherein the routing mechanism is further configured to determine the routing path between the first and second integrated circuit devices by identifying one or more obstacles that block the routing path,
changing specified straying limit criteria that defines a routing region in which the routing path between the first and second integrated circuit devices may be placed to generate changed specified straying limit criteria that defines a modified routing region, and
determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the changed specified straying limit criteria, the routing path between the first and second integrated circuit devices.

33. The system as recited in Claim 29, wherein routing mechanism is further configured to determine the routing path between the first and second integrated circuit devices by identifying one or more obstacles that block the routing path,
determining a set of one or more layer changes to allow the routing path to avoid the one more obstacles, and
determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the set of one or

more layer changes, the routing path between the first and second integrated circuit devices.

34. The method as recited in Claim 1, wherein each routing indicator from the set of one or more routing indicators further specifies a routing direction for the routing path.

35. The computer-readable medium as recited in Claim 24, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

determining a set of one or more bends to be included in the routing path to avoid the one more obstacles, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the set of one or more bends, the routing path between the first and second integrated circuit devices.

36. The computer-readable medium as recited in Claim 24, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

determining one or more portions of the routing path to be ripped up and rerouted, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the one or more

portions of the routing path to be ripped up and rerouted, the routing path between the first and second integrated circuit devices.

37. The computer-readable medium as recited in Claim 36, wherein determining the routing path between the first and second integrated circuit devices further includes

determining one or more portions of one or more other routing paths to be ripped up and rerouted, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators, the one or more portions of the routing path to be ripped up and rerouted and the one or more portions of the one or more other routing paths to be ripped up and rerouted, the routing path between the first and second integrated circuit devices.

38. The computer-readable medium as recited in Claim 24, wherein determining the routing path between the first and second integrated circuit devices further includes

identifying one or more obstacles that block the routing path,

determining one or more portions of one or more other routing paths to be ripped up and rerouted, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the one or more portions of the one or more other routing paths to be ripped up and rerouted, the routing path between the first and second integrated circuit devices.

39. The computer-readable medium as recited in Claim 24, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data and the set of one or more routing indicators, the routing path between the first and second integrated circuit devices, wherein the routing path is routed from the second integrated circuit device to the first integrated circuit device.

40. The computer-readable medium as recited in Claim 24, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

determining one or more locations to employ corner clipping to provide additional space for the routing path, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the one or more locations to employ corner clipping, the routing path between the first and second integrated circuit devices.

41. The computer-readable medium as recited in Claim 24, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

determining one or more integrated circuit layout objects to be moved to provide additional space for the routing path, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and moving the one or more integrated circuit layout objects, the routing path between the first and second integrated circuit devices.

42. The computer-readable medium as recited in Claim 24, wherein determining the routing path between the first and second integrated circuit devices includes

examining data that indicates whether changes can be made to one or more layout objects defined by the integrated circuit layout data to accommodate the routing of the routing path, and

if the data indicates that changes can be made to the one or more layout objects defined by the integrated circuit layout data to accommodate the routing of the routing path, then

making one or more changes to the one or more layout objects defined by the integrated circuit layout data, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the one or more changes made to the one or more layout objects, the routing path between the first and second integrated circuit devices.

43. The computer-readable medium as recited in Claim 42, further comprising one or more additional instructions which, when executed by the one or more processors, cause the one or more processors to generate data that specifies the one or more changes made to the one or more layout objects.

44. The computer-readable medium as recited in Claim 24, wherein determining the routing path between the first and second integrated circuit devices includes

determining a set of one or more routing targets to which the routing path is to be routed, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the set of one or more routing targets, the routing path between the first and second integrated circuit devices.

45. The computer-readable medium as recited in Claim 24, wherein determining the routing path between the first and second integrated circuit devices includes performing one or more design rule checks on one or more portions of the routing path as the routing path is being determined.

46. The computer-readable medium as recited in Claim 45, further comprising one or more additional instructions which, when executed by the one or more processors, cause the one or more processors to perform a design rule check on the updated integrated circuit

layout data, wherein the design rule check does not check one or more layout objects previously checked during determination of the routing path.

47. The computer-readable medium as recited in Claim 24, wherein determining the routing path between the first and second integrated circuit devices includes

extending the routing path a specified amount to generate an extended portion of the routing path, and

selectively performing a design rule check on only the extended portion of the routing path.

48. The computer-readable medium as recited in Claim 24, wherein all attachment and bend angles defined by the updated integrated circuit layout data are multiples of ninety degrees.

49. The computer-readable medium as recited in Claim 24, wherein one or more attachment or bend angles defined by the updated integrated circuit layout data are multiples of other than ninety degrees.

50. A computer-readable medium carrying one or more sequences of one or more instructions for automatically verifying an integrated circuit layout, the one or more sequences of one or more instructions including instructions which, when executed by one or more processors, cause the one or more processors to perform the steps of:

receiving integrated circuit layout data that defines a set of two or more layout objects contained in the integrated circuit layout;

performing a first design rule check on a layout object from the set of two or more layout objects by evaluating the layout object against specified design criteria;

changing one or more values defined by the specified design criteria to generate updated specified design criteria, wherein the changing of the one or more values is performed after a specified amount of time has elapsed and is made with respect to either the layout object or one or more other layout objects from the set of two or more layout objects; and

performing a second design rule check on the layout object by evaluating the layout object against the updated specified design criteria.

51. A computer-readable medium carrying one or more sequences of one or more instructions for automatically routing an integrated circuit, the one or more sequences of one or more instructions including instructions which, when executed by one or more processors, cause the one or more processors to perform the steps of:

receiving integrated circuit layout data that defines a set of two or more integrated circuit devices to be included in the integrated circuit;

receiving integrated circuit connection data that specifies one or more electrical connections to be made between the integrated circuit devices;

determining, based upon the integrated circuit layout data and the integrated circuit connection data, a set of two or more join points that are to be electrically connected, wherein each join point from the set of two or more join points has an

associated set of specified design criteria that control attachment of routing paths thereto;

determining, based upon the integrated circuit layout data and the set of two or more join points, one or more routing paths to connect the set of two or more join points, wherein the one or more routing paths satisfy the specified design criteria associated with the set of two or more join points; and

updating the integrated circuit layout data to generate updated integrated circuit layout data that reflects the one or more routing paths.

52. A computer-readable medium carrying one or more sequences of one or more instructions for automatically routing an integrated circuit, the one or more sequences of one or more instructions including instructions which, when executed by one or more processors, cause the one or more processors to perform the steps of:

receiving integrated circuit layout data that defines a set of two or more integrated circuit devices to be included in the integrated circuit;

receiving integrated circuit connection data that specifies one or more electrical connections to be made between the integrated circuit devices;

determining, based upon the integrated circuit layout data and the integrated circuit connection data, a routing path between first and second integrated circuit devices that satisfies specified design criteria, wherein determining the routing path between the first and second integrated circuit devices includes

determining whether the distance to be routed for a portion of the routing path exceeds a specified distance, and

if the distance to be routed for the portion of the routing path does not exceed the specified distance, then routing the portion of the routing path in a single step; and

updating the integrated circuit layout data to generate updated integrated circuit layout data that reflects the routing path between the first and second integrated circuit devices.

53. The system as recited in Claim 29, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

determining a set of one or more bends to be included in the routing path to avoid the one more obstacles, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the set of one or more bends, the routing path between the first and second integrated circuit devices.

54. The system as recited in Claim 29, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

determining one or more portions of the routing path to be ripped up and rerouted, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the one or more

portions of the routing path to be ripped up and rerouted, the routing path between the first and second integrated circuit devices.

55. The system as recited in Claim 54, wherein determining the routing path between the first and second integrated circuit devices further includes

determining one or more portions of one or more other routing paths to be ripped up and rerouted, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators, the one or more portions of the routing path to be ripped up and rerouted and the one or more portions of the one or more other routing paths to be ripped up and rerouted, the routing path between the first and second integrated circuit devices.

56. The system as recited in Claim 29, wherein determining the routing path between the first and second integrated circuit devices further includes

identifying one or more obstacles that block the routing path,

determining one or more portions of one or more other routing paths to be ripped up and rerouted, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the one or more portions of the one or more other routing paths to be ripped up and rerouted, the routing path between the first and second integrated circuit devices.

57. The system as recited in Claim 29, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data and the set of one or more routing indicators, the routing path between the first and second integrated circuit devices, wherein the routing path is routed from the second integrated circuit device to the first integrated circuit device.

58. The system as recited in Claim 29, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

determining one or more locations to employ corner clipping to provide additional space for the routing path, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the one or more locations to employ corner clipping, the routing path between the first and second integrated circuit devices.

59. The system as recited in Claim 29, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

determining one or more integrated circuit layout objects to be moved to provide additional space for the routing path, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and moving the one or more integrated circuit layout objects, the routing path between the first and second integrated circuit devices.

60. The system as recited in Claim 29, wherein determining the routing path between the first and second integrated circuit devices includes

examining data that indicates whether changes can be made to one or more layout objects defined by the integrated circuit layout data to accommodate the routing of the routing path, and

if the data indicates that changes can be made to the one or more layout objects defined by the integrated circuit layout data to accommodate the routing of the routing path, then

making one or more changes to the one or more layout objects defined by the integrated circuit layout data, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the one or more changes made to the one or more layout objects, the routing path between the first and second integrated circuit devices.

61. The system as recited in Claim 60, wherein the routing mechanism is further configured to generate data that specifies the one or more changes made to the one or more layout objects.

62. The system as recited in Claim 29, wherein determining the routing path between the first and second integrated circuit devices includes

determining a set of one or more routing targets to which the routing path is to be routed, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the set of one or more routing targets, the routing path between the first and second integrated circuit devices.

63. The system as recited in Claim 29, wherein determining the routing path between the first and second integrated circuit devices includes performing one or more design rule checks on one or more portions of the routing path as the routing path is being determined.

64. The system as recited in Claim 63, wherein the routing mechanism is further configured to perform a design rule check on the updated integrated circuit layout data, wherein the design rule check does not check one or more layout objects previously checked during determination of the routing path.

65. The system as recited in Claim 29, wherein determining the routing path between the first and second integrated circuit devices includes

extending the routing path a specified amount to generate an extended portion of the routing path, and

selectively performing a design rule check on only the extended portion of the routing path.

66. The system as recited in Claim 29, wherein all attachment and bend angles defined by the updated integrated circuit layout data are multiples of ninety degrees.

67. The system as recited in Claim 29, wherein one or more attachment or bend angles defined by the updated integrated circuit layout data are multiples of other than ninety degrees.

TABLE 1

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TO: Examiner A.M. Thompson	FROM: Edward A. Becker
COMPANY: USPTO Group Art Unit 2825	DATE: SEPTEMBER 10, 2001
FAX NUMBER: 703-305-3431	TOTAL NO. OF PAGES INCLUDING COVER: 31
PHONE NUMBER: 703-305-7441	SENDER'S REFERENCE NUMBER: 50265-0018
RE: Response to Final Office Action	YOUR REFERENCE NUMBER: 09/421,437

☑ URGENT ☐ FOR REVIEW ☐ PLEASE COMMENT ☐ PLEASE REPLY ☐ PLEASE RECYCLE

NOTES/COMMENTS:

PLEASE DELIVER IMMEDIATELY TO EXAMINER A.M. THOMPSON.

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Docket No. 50265-0018

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	) Group Art Unit: 2825
David C. CHAPMAN	) Examiner: A. Thompson
Serial No. 09/421,437	)
Filed: October 19, 1999	)

For: APPROACH FOR ROUTING AN INTEGRATED CIRCUIT

Box AF
Commissioner for Patents
Washington, D.C. 20231

AMENDMENT AFTER FINAL REJECTION

Sir:

In response to the Final Office Action mailed July 11, 2001, please amend the application referenced above as indicated hereinafter. Pursuant to updated rule 37 C.F.R. § 1.121, the amended claim is provided in "clean form" below and a complete set of marked up claims showing the deletions and additions in the amended claim is provided on separate pages after this amendment.

21. (ONCE AMENDED) A method for automatically verifying an integrated circuit layout, the method comprising the computer-implemented steps of:

receiving integrated circuit layout data that defines a set of two or more layout objects contained in the integrated circuit layout;

performing a first design rule check on a layout object from the set of two or more layout objects by evaluating the layout object against specified design criteria;

changing one or more values defined by the specified design criteria to generate updated specified design criteria, wherein the changing of the one or more values is performed after a specified amount of time has elapsed and is made with respect to only the layout object; and

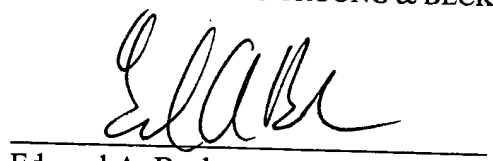
performing a second design rule check on the layout object by evaluating the layout object against the updated specified design criteria.

REMARKS

By this amendment, Claim 21 has been amended. Hence, Claims 1-67 are pending in this application. The amendment to Claim 21 does not add any new matter to this application. Applicant respectfully submits that the amendment to Claim 21 places Claim 21 in better form for consideration on appeal and the entering of the amendment is therefore respectfully requested.

If there are any additional charges, please charge them to Deposit Account No. 50-1302.

Respectfully submitted,
HICKMAN PALERMO TRUONG & BECKER LLP



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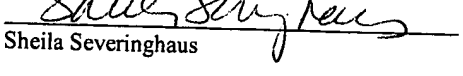
on September 10, 2001 by 
Sheila Severinghaus

MARKED UP VERSIONS OF CLAIMS

1. (NOT AMENDED) A method for automatically routing an integrated circuit, the method comprising the computer-implemented steps of:

receiving integrated circuit layout data that defines a set of two or more integrated circuit devices to be included in the integrated circuit;

receiving integrated circuit connection data that specifies one or more electrical connections to be made between the integrated circuit devices;

determining, based upon the integrated circuit layout data and the integrated circuit connection data, a set of one or more routing indicators that specify a set of one or more preferable intermediate routing locations through which a routing path is to be located to connect first and second integrated circuit devices from the set of two or more integrated circuit devices;

determining, based upon the integrated circuit layout data, the integrated circuit connection data and the set of one or more routing indicators, the routing path between the first and second integrated circuit devices, wherein the routing path satisfies specified design criteria; and

updating the integrated circuit layout data to generate updated integrated circuit layout data that reflects the routing path between the first and second integrated circuit devices.

2. (NOT AMENDED) The method as recited in Claim 1, wherein determining the routing path includes determining, based upon the integrated circuit layout data, the integrated circuit connection data, bias direction criteria and straying limit criteria, the routing path between the first and second integrated circuit devices, wherein the bias direction criteria specifies a preferred routing direction for a

routing path between first and second integrated circuit devices from the set of two or more integrated circuit devices and the straying limit criteria defines a routing region in which the routing path between the first and second integrated circuit devices may be placed.

3. (NOT AMENDED) The method as recited in Claim 1, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

determining, based upon the integrated circuit layout data, the integrated circuit connection data and the one or more obstacles, one or more additional routing indicators that specify one or more preferable routing locations through which the routing path is to be located to avoid the one or more obstacles, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the one or more additional routing indicators, the routing path between the first and second integrated circuit devices.

4. (NOT AMENDED) The method as recited in Claim 1, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

changing specified straying limit criteria that defines a routing region in which the routing path between the first and second integrated circuit devices may be placed to generate changed specified straying limit criteria that defines a modified routing region, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the changed

specified straying limit criteria, the routing path between the first and second integrated circuit devices.

5. (NOT AMENDED) The method as recited in Claim 1, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

determining a set of one or more layer changes to allow the routing path to avoid the one more obstacles, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the set of one or more layer changes, the routing path between the first and second integrated circuit devices.

6. (NOT AMENDED) The method as recited in Claim 1, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

determining a set of one or more bends to be included in the routing path to avoid the one more obstacles, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the set of one or more bends, the routing path between the first and second integrated circuit devices.

7. (NOT AMENDED) The method as recited in Claim 1, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

determining one or more portions of the routing path to be ripped up and rerouted, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the one or more portions of the routing path to be ripped up and rerouted, the routing path between the first and second integrated circuit devices.

8. (NOT AMENDED) The method as recited in Claim 7, wherein determining the routing path between the first and second integrated circuit devices further includes

determining one or more portions of one or more other routing paths to be ripped up and rerouted, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators, the one or more portions of the routing path to be ripped up and rerouted and the one or more portions of the one or more other routing paths to be ripped up and rerouted, the routing path between the first and second integrated circuit devices.

9. (NOT AMENDED) The method as recited in Claim 1, wherein determining the routing path between the first and second integrated circuit devices further includes

identifying one or more obstacles that block the routing path,

determining one or more portions of one or more other routing paths to be ripped up and rerouted, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the one or

more portions of the one or more other routing paths to be ripped up and rerouted, the routing path between the first and second integrated circuit devices.

10. (NOT AMENDED) The method as recited in Claim 1, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data and the set of one or more routing indicators, the routing path between the first and second integrated circuit devices, wherein the routing path is routed from the second integrated circuit device to the first integrated circuit device.

11. (NOT AMENDED) The method as recited in Claim 1, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

determining one or more locations to employ corner clipping to provide additional space for the routing path, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the one or more locations to employ corner clipping, the routing path between the first and second integrated circuit devices.

12. (NOT AMENDED) The method as recited in Claim 1, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

determining one or more integrated circuit layout objects to be moved to provide additional space for the routing path, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and moving the one or more integrated circuit layout objects, the routing path between the first and second integrated circuit devices.

13. (NOT AMENDED) The method as recited in Claim 1, wherein determining the routing path between the first and second integrated circuit devices includes

examining data that indicates whether changes can be made to one or more layout objects defined by the integrated circuit layout data to accommodate the routing of the routing path, and

if the data indicates that changes can be made to the one or more layout objects defined by the integrated circuit layout data to accommodate the routing of the routing path, then

making one or more changes to the one or more layout objects defined by the integrated circuit layout data, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the one or more changes made to the one or more layout objects, the routing path between the first and second integrated circuit devices.

14. (NOT AMENDED) The method as recited in Claim 13, further comprising generating data that specifies the one or more changes made to the one or more layout objects.

15. (NOT AMENDED) The method as recited in Claim 1, wherein determining the routing path between the first and second integrated circuit devices includes determining a set of one or more routing targets to which the routing path is to be routed, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the set of one or more routing targets, the routing path between the first and second integrated circuit devices.

16. (NOT AMENDED) The method as recited in Claim 1, wherein determining the routing path between the first and second integrated circuit devices includes performing one or more design rule checks on one or more portions of the routing path as the routing path is being determined.

17. (NOT AMENDED) The method as recited in Claim 16, further comprising performing a design rule check on the updated integrated circuit layout data, wherein the design rule check does not check one or more layout objects previously checked during determination of the routing path.

18. (NOT AMENDED) The method as recited in Claim 1, wherein determining the routing path between the first and second integrated circuit devices includes extending the routing path a specified amount to generate an extended portion of the routing path, and

selectively performing a design rule check on only the extended portion of the routing path.

19. (NOT AMENDED) The method as recited in Claim 1, wherein all attachment and bend angles defined by the updated integrated circuit layout data are multiples of ninety degrees.

20. (NOT AMENDED) The method as recited in Claim 1, wherein one or more attachment or bend angles defined by the updated integrated circuit layout data are multiples of other than ninety degrees.

21. (ONCE AMENDED) A method for automatically verifying an integrated circuit layout, the method comprising the computer-implemented steps of:

receiving integrated circuit layout data that defines a set of two or more layout objects contained in the integrated circuit layout;

performing a first design rule check on a layout object from the set of two or more layout objects by evaluating the layout object against specified design criteria;

changing one or more values defined by the specified design criteria to generate updated specified design criteria, wherein the changing of the one or more values is performed after a specified amount of time has elapsed and is made with respect to [either] only the layout object; [object or one or more other layout objects from the set of two or more layout objects;] and

performing a second design rule check on the layout object by evaluating the layout object against the updated specified design criteria.

22. (NOT AMENDED) A method for automatically routing an integrated circuit, the method comprising the computer-implemented steps of:

receiving integrated circuit layout data that defines a set of two or more integrated circuit devices to be included in the integrated circuit;

receiving integrated circuit connection data that specifies one or more electrical connections to be made between the integrated circuit devices;

determining, based upon the integrated circuit layout data and the integrated circuit connection data, a set of two or more join points that are to be electrically connected, wherein each join point from the set of two or more join points has an associated set of specified design criteria that control attachment of routing paths thereto;

determining, based upon the integrated circuit layout data and the set of two or more join points, one or more routing paths to connect the set of two or more join points, wherein the one or more routing paths satisfy the specified design criteria associated with the set of two or more join points; and

updating the integrated circuit layout data to generate updated integrated circuit layout data that reflects the one or more routing paths.

23. (NOT AMENDED) A method for automatically routing an integrated circuit, the method comprising the computer-implemented steps of:

receiving integrated circuit layout data that defines a set of two or more integrated circuit devices to be included in the integrated circuit;

receiving integrated circuit connection data that specifies one or more electrical connections to be made between the integrated circuit devices;

determining, based upon the integrated circuit layout data and the integrated circuit connection data, a routing path between first and second integrated circuit devices that satisfies specified design criteria, wherein determining the routing path between the first and second integrated circuit devices includes

determining whether the distance to be routed for a portion of the routing path exceeds a specified distance, and

if the distance to be routed for the portion of the routing path does not exceed the specified distance, then routing the portion of the routing path in a single step; and

updating the integrated circuit layout data to generate updated integrated circuit layout data that reflects the routing path between the first and second integrated circuit devices.

24. (NOT AMENDED) A computer-readable medium carrying one or more sequences of one or more instructions for automatically routing an integrated circuit, the one or more sequences of one or more instructions including instructions which, when executed by one or more processors, cause the one or more processors to perform the steps of:

receiving integrated circuit layout data that defines a set of two or more integrated circuit devices to be included in the integrated circuit;

receiving integrated circuit connection data that specifies one or more electrical connections to be made between the integrated circuit devices;

determining, based upon the integrated circuit layout data and the integrated circuit connection data, a set of one or more routing indicators that specify a set of one or more preferable intermediate routing locations through which a routing path is to be located to connect first and second integrated circuit devices from the set of two or more integrated circuit devices;

determining, based upon the integrated circuit layout data, the integrated circuit connection data and the set of one or more routing indicators, the routing path between the first and second integrated circuit devices, wherein the routing path satisfies specified design criteria; and

updating the integrated circuit layout data to generate updated integrated circuit layout data that reflects the routing path between the first and second integrated circuit devices.

25. (NOT AMENDED) The computer-readable medium as recited in Claim 24, wherein determining the routing path includes determining, based upon the integrated circuit layout data, the integrated circuit connection data, bias direction criteria and straying limit criteria, the routing path between the first and second integrated circuit devices, wherein the bias direction criteria specifies a preferred routing direction for a routing path between first and second integrated circuit devices from the set of two or more integrated circuit devices and the straying limit criteria defines a routing region in which the routing path between the first and second integrated circuit devices may be placed.

26. (NOT AMENDED) The computer-readable medium as recited in Claim 24, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

determining, based upon the integrated circuit layout data, the integrated circuit connection data and the one or more obstacles, one or more additional routing indicators that specify one or more preferable routing locations through which the routing path is to be located to avoid the one or more obstacles, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the one or more additional routing indicators, the routing path between the first and second integrated circuit devices.

27. (NOT AMENDED) The computer-readable medium as recited in Claim 24, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

changing specified straying limit criteria that defines a routing region in which the routing path between the first and second integrated circuit devices may be placed to generate changed specified straying limit criteria that defines a modified routing region, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the changed specified straying limit criteria, the routing path between the first and second integrated circuit devices.

28. (NOT AMENDED) The computer-readable medium as recited in Claim 24, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

determining a set of one or more layer changes to allow the routing path to avoid the one more obstacles, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the set of one or more layer changes, the routing path between the first and second integrated circuit devices.

29. (NOT AMENDED) A system for automatically routing an integrated circuit, the system comprising:

a data storage mechanism having stored therein

integrated circuit layout data that defines a set of two or more integrated circuit devices to be included in the integrated circuit, and

integrated circuit connection data that specifies one or more electrical connections to be made between the integrated circuit devices; and

a routing mechanism communicatively coupled to the data storage mechanism, the routing mechanism being configured to

determine, based upon the integrated circuit layout data and the integrated circuit connection data, a set of one or more routing indicators that specify a set of one or more preferable intermediate routing locations through which a routing path is to be located to connect first and second integrated circuit devices from the set of two or more integrated circuit devices,

determine, based upon the integrated circuit layout data, the integrated circuit connection data and the set of one or more routing indicators, the routing path between the first and second integrated circuit devices, wherein the routing path satisfies specified design criteria, and

update the integrated circuit layout data to generate updated integrated circuit layout data that reflects the routing path between the first and second integrated circuit devices.

30. (NOT AMENDED) The system as recited in Claim 29, wherein the routing mechanism is further configured to determine the routing path by determining, based upon the integrated circuit layout data, the integrated circuit connection data, bias direction criteria and straying limit criteria, the routing path between the first and second integrated circuit devices, wherein the bias direction criteria

specifies a preferred routing direction for a routing path between first and second integrated circuit devices from the set of two or more integrated circuit devices and the straying limit criteria defines a routing region in which the routing path between the first and second integrated circuit devices may be placed.

31. (NOT AMENDED) The system as recited in Claim 29, wherein the routing mechanism is further configured to determine the routing path between the first and second integrated circuit devices by

identifying one or more obstacles that block the routing path,

determining, based upon the integrated circuit layout data, the integrated circuit connection data and the one or more obstacles, one or more additional routing indicators that specify one or more preferable routing locations through which the routing path is to be located to avoid the one or more obstacles, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the one or more additional routing indicators, the routing path between the first and second integrated circuit devices.

32. (NOT AMENDED) The system as recited in Claim 29, wherein the routing mechanism is further configured to determine the routing path between the first and second integrated circuit devices by

identifying one or more obstacles that block the routing path,

changing specified straying limit criteria that defines a routing region in which the routing path between the first and second integrated circuit devices may be placed to generate changed specified straying limit criteria that defines a modified routing region, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the changed specified straying limit criteria, the routing path between the first and second integrated circuit devices.

33. (NOT AMENDED) The system as recited in Claim 29, wherein routing mechanism is further configured to determine the routing path between the first and second integrated circuit devices by

identifying one or more obstacles that block the routing path,

determining a set of one or more layer changes to allow the routing path to avoid the one more obstacles, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the set of one or more layer changes, the routing path between the first and second integrated circuit devices.

34. (NOT AMENDED) The method as recited in Claim 1, wherein each routing indicator from the set of one or more routing indicators further specifies a routing direction for the routing path.

35. (NOT AMENDED) The computer-readable medium as recited in Claim 24, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

determining a set of one or more bends to be included in the routing path to avoid the one more obstacles, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the set of one or more bends, the routing path between the first and second integrated circuit devices.

36. (NOT AMENDED) The computer-readable medium as recited in Claim 24, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

determining one or more portions of the routing path to be ripped up and rerouted, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the one or more portions of the routing path to be ripped up and rerouted, the routing path between the first and second integrated circuit devices.

37. (NOT AMENDED) The computer-readable medium as recited in Claim 36, wherein determining the routing path between the first and second integrated circuit devices further includes

determining one or more portions of one or more other routing paths to be ripped up and rerouted, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators, the one or more portions of the routing path to be ripped up and rerouted and the one or more portions of the one or more other routing paths to be ripped up and rerouted, the routing path between the first and second integrated circuit devices.

38. (NOT AMENDED) The computer-readable medium as recited in Claim 24, wherein determining the routing path between the first and second integrated circuit devices further includes

identifying one or more obstacles that block the routing path,

determining one or more portions of one or more other routing paths to be ripped up and rerouted, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the one or more portions of the one or more other routing paths to be ripped up and rerouted, the routing path between the first and second integrated circuit devices.

39. (NOT AMENDED) The computer-readable medium as recited in Claim 24, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data and the set of one or more routing indicators, the routing path between the first and second integrated circuit devices, wherein the routing path is routed from the second integrated circuit device to the first integrated circuit device.

40. (NOT AMENDED) The computer-readable medium as recited in Claim 24, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

determining one or more locations to employ corner clipping to provide additional space for the routing path, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the one or more locations to employ corner clipping, the routing path between the first and second integrated circuit devices.

41. (NOT AMENDED) The computer-readable medium as recited in Claim 24, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

determining one or more integrated circuit layout objects to be moved to provide additional space for the routing path, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and moving the one or more integrated circuit layout objects, the routing path between the first and second integrated circuit devices.

42. (NOT AMENDED) The computer-readable medium as recited in Claim 24, wherein determining the routing path between the first and second integrated circuit devices includes

examining data that indicates whether changes can be made to one or more layout objects defined by the integrated circuit layout data to accommodate the routing of the routing path, and

if the data indicates that changes can be made to the one or more layout objects defined by the integrated circuit layout data to accommodate the routing of the routing path, then

making one or more changes to the one or more layout objects defined by the integrated circuit layout data, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the one or more changes made to the one or more layout objects, the routing path between the first and second integrated circuit devices.

43. (NOT AMENDED) The computer-readable medium as recited in Claim 42, further comprising one or more additional instructions which, when executed by the one or more processors, cause the one or more processors to generate data that specifies the one or more changes made to the one or more layout objects.

44. (NOT AMENDED) The computer-readable medium as recited in Claim 24, wherein determining the routing path between the first and second integrated circuit devices includes

determining a set of one or more routing targets to which the routing path is to be routed, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the set of one or more routing targets, the routing path between the first and second integrated circuit devices.

45. (NOT AMENDED) The computer-readable medium as recited in Claim 24, wherein determining the routing path between the first and second integrated circuit devices includes performing one or more design rule checks on one or more portions of the routing path as the routing path is being determined.

46. (NOT AMENDED) The computer-readable medium as recited in Claim 45, further comprising one or more additional instructions which, when executed by the one or more processors, cause the one or more processors to perform a design rule check on the updated integrated circuit layout data, wherein the design rule check does not check one or more layout objects previously checked during determination of the routing path.

47. (NOT AMENDED) The computer-readable medium as recited in Claim 24, wherein determining the routing path between the first and second integrated circuit devices includes

extending the routing path a specified amount to generate an extended portion of the routing path, and

selectively performing a design rule check on only the extended portion of the routing path.

48. (NOT AMENDED) The computer-readable medium as recited in Claim 24, wherein all attachment and bend angles defined by the updated integrated circuit layout data are multiples of ninety degrees.

49. (NOT AMENDED) The computer-readable medium as recited in Claim 24, wherein one or more attachment or bend angles defined by the updated integrated circuit layout data are multiples of other than ninety degrees.

50. (NOT AMENDED) A computer-readable medium carrying one or more sequences of one or more instructions for automatically verifying an integrated circuit layout, the one or more sequences of one or more instructions including

instructions which, when executed by one or more processors, cause the one or more processors to perform the steps of:

receiving integrated circuit layout data that defines a set of two or more layout objects contained in the integrated circuit layout;

performing a first design rule check on a layout object from the set of two or more layout objects by evaluating the layout object against specified design criteria;

changing one or more values defined by the specified design criteria to generate updated specified design criteria, wherein the changing of the one or more values is performed after a specified amount of time has elapsed and is made with respect to either the layout object or one or more other layout objects from the set of two or more layout objects; and

performing a second design rule check on the layout object by evaluating the layout object against the updated specified design criteria.

51. (NOT AMENDED) A computer-readable medium carrying one or more sequences of one or more instructions for automatically routing an integrated circuit, the one or more sequences of one or more instructions including instructions which, when executed by one or more processors, cause the one or more processors to perform the steps of:

receiving integrated circuit layout data that defines a set of two or more integrated circuit devices to be included in the integrated circuit;

receiving integrated circuit connection data that specifies one or more electrical connections to be made between the integrated circuit devices;

determining, based upon the integrated circuit layout data and the integrated circuit connection data, a set of two or more join points that are to be electrically connected, wherein each join point from the set of two or more

join points has an associated set of specified design criteria that control attachment of routing paths thereto;

determining, based upon the integrated circuit layout data and the set of two or more join points, one or more routing paths to connect the set of two or more join points, wherein the one or more routing paths satisfy the specified design criteria associated with the set of two or more join points; and

updating the integrated circuit layout data to generate updated integrated circuit layout data that reflects the one or more routing paths.

52. (NOT AMENDED) A computer-readable medium carrying one or more sequences of one or more instructions for automatically routing an integrated circuit, the one or more sequences of one or more instructions including instructions which, when executed by one or more processors, cause the one or more processors to perform the steps of:

receiving integrated circuit layout data that defines a set of two or more integrated circuit devices to be included in the integrated circuit;

receiving integrated circuit connection data that specifies one or more electrical connections to be made between the integrated circuit devices;

determining, based upon the integrated circuit layout data and the integrated circuit connection data, a routing path between first and second integrated circuit devices that satisfies specified design criteria, wherein determining the routing path between the first and second integrated circuit devices includes

determining whether the distance to be routed for a portion of the routing path exceeds a specified distance, and

if the distance to be routed for the portion of the routing path does not exceed the specified distance, then routing the portion of the routing path in a single step; and

updating the integrated circuit layout data to generate updated integrated circuit layout data that reflects the routing path between the first and second integrated circuit devices.

53. (NOT AMENDED) The system as recited in Claim 29, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

determining a set of one or more bends to be included in the routing path to avoid the one more obstacles, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the set of one or more bends, the routing path between the first and second integrated circuit devices.

54. (NOT AMENDED) The system as recited in Claim 29, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

determining one or more portions of the routing path to be ripped up and rerouted, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the one or more portions of the routing path to be ripped up and rerouted, the routing path between the first and second integrated circuit devices.

55. (NOT AMENDED) The system as recited in Claim 54, wherein determining the routing path between the first and second integrated circuit devices further includes

determining one or more portions of one or more other routing paths to be ripped up and rerouted, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators, the one or more portions of the routing path to be ripped up and rerouted and the one or more portions of the one or more other routing paths to be ripped up and rerouted, the routing path between the first and second integrated circuit devices.

56. (NOT AMENDED) The system as recited in Claim 29, wherein determining the routing path between the first and second integrated circuit devices further includes

identifying one or more obstacles that block the routing path,

determining one or more portions of one or more other routing paths to be ripped up and rerouted, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the one or more portions of the one or more other routing paths to be ripped up and rerouted, the routing path between the first and second integrated circuit devices.

57. (NOT AMENDED) The system as recited in Claim 29, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data and the set of one or more routing indicators, the routing path between the first and second integrated circuit devices, wherein the routing path is routed from the second integrated circuit device to the first integrated circuit device.

58. (NOT AMENDED) The system as recited in Claim 29, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

determining one or more locations to employ corner clipping to provide additional space for the routing path, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the one or more locations to employ corner clipping, the routing path between the first and second integrated circuit devices.

59. (NOT AMENDED) The system as recited in Claim 29, wherein determining the routing path between the first and second integrated circuit devices includes

identifying one or more obstacles that block the routing path,

determining one or more integrated circuit layout objects to be moved to provide additional space for the routing path, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and moving the one or more integrated circuit layout objects, the routing path between the first and second integrated circuit devices.

60. (NOT AMENDED) The system as recited in Claim 29, wherein determining the routing path between the first and second integrated circuit devices includes

examining data that indicates whether changes can be made to one or more layout objects defined by the integrated circuit layout data to accommodate the routing of the routing path, and

if the data indicates that changes can be made to the one or more layout objects defined by the integrated circuit layout data to accommodate the routing of the routing path, then

making one or more changes to the one or more layout objects defined by the integrated circuit layout data, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the one or more changes made to the one or more layout objects, the routing path between the first and second integrated circuit devices.

61. (NOT AMENDED) The system as recited in Claim 60, wherein the routing mechanism is further configured to generate data that specifies the one or more changes made to the one or more layout objects.

62. (NOT AMENDED) The system as recited in Claim 29, wherein determining the routing path between the first and second integrated circuit devices includes

determining a set of one or more routing targets to which the routing path is to be routed, and

determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the set of

one or more routing targets, the routing path between the first and second integrated circuit devices.

63. (NOT AMENDED) The system as recited in Claim 29, wherein determining the routing path between the first and second integrated circuit devices includes performing one or more design rule checks on one or more portions of the routing path as the routing path is being determined.

64. (NOT AMENDED) The system as recited in Claim 63, wherein the routing mechanism is further configured to perform a design rule check on the updated integrated circuit layout data, wherein the design rule check does not check one or more layout objects previously checked during determination of the routing path.

65. (NOT AMENDED) The system as recited in Claim 29, wherein determining the routing path between the first and second integrated circuit devices includes extending the routing path a specified amount to generate an extended portion of the routing path, and
selectively performing a design rule check on only the extended portion of the routing path.

66. (NOT AMENDED) The system as recited in Claim 29, wherein all attachment and bend angles defined by the updated integrated circuit layout data are multiples of ninety degrees.

67. (NOT AMENDED) The system as recited in Claim 29, wherein one or more attachment or bend angles defined by the updated integrated circuit layout data are multiples of other than ninety degrees.